Claims

[c1] 1. A method for designing wiring in a multilayered substrate so as to limit a temperature gradient in said wiring, comprising the steps of:

providing an initial wiring design in which the multilayered substrate comprises layers stacked in a Y direction, wherein each layer of said layers has its length oriented in a X direction that is orthogonal to the Y direction, wherein a first electrically conductive wire within a first layer of said layers has its length oriented in the X direction, wherein in the initial wiring design the first wire has a spatially nonuniform temperature distribution T(X) along its length for an assumed current density J1 in the first wire such that the first wire has a mean time to failure MTF1 at the current density J1; and

altering the initial wiring design to reduce the magnitude of a temperature gradient dT(X)/dX along the length of the first wire for a current density J2 not less than J1 in the first wire, wherein the altering does not include changing a cross sectional area of the first wire, wherein the altering includes electrically and thermally coupling the first wire to a second electrically conductive wire in the first layer by an electrically and thermally conductive structure that exists outside of the first layer and adjusting the width distribution of the second wire in a Z direction that is orthogonal to the X and Y directions, wherein the first and second wires do not physically touch each other, and wherein said adjusting controls a temperature in the second wire so as to cause the second wire to act as a heat source or heat sink to the first wire.

[c2] The method of claim 1, further comprising the steps of:

following said altering: measuring T(X) along the length of the first wire; determining in accordance with an acceptance criterion whether dT(X)/dX inferred from the measured T(X) is acceptable; and if dT(X)/dX is not determined by said determining to be acceptable, then iteratively re-executing the altering, measuring, and determining steps until dT(X)/dX is determined by said determining to be acceptable.

[c3] The method of claim 1, wherein the first wire is coupled to a current source.

[c4] 4. The method of claim 1, wherein J_2 exceeds J_1 and the altering does not essentially change the mean time to failure of the first wire from MTF1.

[c5] 5. The method of claim 1, wherein J_2 is about equal to J_1 and the altering changes the mean time to failure of the first wire to MTF2 such that MTF2 > MTF1.

[c6] 6. The method of claim 1, wherein the electrically and thermally conductive structure includes:

a first electrically and thermally conductive via oriented in the Y direction such that the first via is electrically and thermally connected to the first wire;

a second electrically and thermally conductive via oriented in the Y direction such that the second via is electrically and thermally connected to the second wire; and

a third electrically conductive wire in a second layer of said layers, wherein the third wire has its length oriented in the X direction, wherein the second layer is above or below the first layer, and wherein the third

wire is electrically and thermally connected to the first and second vias.

[c7] The method of claim 6, wherein the altering includes removing an intermediate portion of the first wire so as to generate remaining first and second portions of the first wire not physically touching each other, wherein the second portion of the first wire comprises the second wire, and wherein electrically and thermally connecting the first wire to the first via includes electrically and thermally connecting the first portion of the first wire to the first via.

[c8] The method of claim 6, wherein the second wire is an additional wire that does not comprise any portion of the first wire.

[c9] The method of claim 6, wherein the second layer is disposed between the first layer and a device layer of the substrate, and wherein the second wire is a heat sink to the first wire at the current density J2 in the first wire.

[c10] 10.The method of claim 9, wherein the electrical resistivity of the first wire is less than the electrical resistivity of the second wire.

[c11] 11.The method of claim 6, wherein the first layer is disposed between the second layer and a device layer of the substrate, and wherein the second wire is a heat source to the first wire at the current density J_2 in the first wire.

[c12] 12. The method of claim 11, wherein the electrical resistivity of the first wire exceeds the electrical resistivity of the second wire.

[c13] 13. The method of claim 6, wherein the altering further includes modifying a width of the third wire in the Z direction.

[c14] 14.The method of claim 6, wherein the altering further includes modifying a cross sectional area of at least one of the first and second vias.

[c15] 15.The method of claim 1, wherein the substrate further comprises a device layer, wherein the altering further comprises adding a thermally conductive member in a thermally conductive layer of the substrate, wherein the thermally conductive layer is above or below the first layer, wherein the thermally conductive member and the device layer are thermally coupled to each other by a dielectric layer disposed between the first wire and the thermally conductive member and by at least one thermally conductive via disposed between the thermally conductive member and the device layer, wherein the dielectric layer has a sufficiently small thickness in the Y direction that permits conductive heat transfer through the thickness of the dielectric layer, and wherein the thermally conductive member does not carry an electric current.

[c16] 16. The method of claim 15, wherein the thermally conductive layer is disposed between the first layer and the device layer.

[c17] 17. The method of claim 15, wherein the first layer is disposed between the thermally conductive layer and the device layer.

[c18] 18. The method of claim 15, wherein the at least one thermally conductive via is in mechanical contact with a portion of the device layer that does not include an active electronic device.

[c19] 19. An electronic structure for limiting a temperature gradient in wiring within a multilayered substrate, said electronic structure comprising a multilayered substrate having layers stacked in a Y direction, wherein each layer of said layers has its length oriented in a X direction that is orthogonal to the Y direction, wherein first and second electrically conductive wires within a first layer of said layers have their respective lengths oriented in the X direction, wherein the first wire is electrically and thermally coupled to the second wire by an electrically and thermally conductive structure that exists outside of the first layer, wherein the first and second wires do not physically touch each other, wherein the first wire is adapted to have a temperature distribution T(X) along its length at a given current density J in the first wire, wherein a width distribution of the second wire in a Z direction that is orthogonal to the X and Y directions is tailored so as to limit the temperature gradient dT(X)/dX to be below a real positive number , for all values of X, and wherein , is predetermined to be sufficiently small so as to substantially mitigate adverse effects of electromigration in the first wire.

[c20] 20. The electronic structure of claim 19, wherein the first wire is coupled to a current source.

[c21] 21. The electronic structure of claim 19, wherein the mean time to failure of the first wire at the current density J is about minimal with respect to variations in the width of the second wire.

[c22] 22.The electronic structure of claim 19, wherein the electrically and thermally conductive structure includes:

a first electrically and thermally conductive via oriented in the Y direction such that the first via is electrically and thermally connected to the first wire;

a second electrically and thermally conductive via oriented in the Y direction such that the second via is electrically and thermally connected to the second wire; and

a third electrically conductive wire in a second layer of said layers, wherein the third wire has its length oriented in the X direction, wherein the second layer is above or below the first layer, and wherein the third wire is electrically and thermally connected to the first and second vias.

[c23] 23. The electronic structure of claim 22, wherein the second layer is disposed between the first layer and a device layer of the substrate, and wherein the second wire is a heat sink to the first wire at the current density J in the first wire.

[c24] 24. The electronic structure of claim 23, wherein the electrical resistivity of the first wire is less than the electrical resistivity of the second wire.

[c25] 25. The electronic structure of claim 22, wherein the first layer is disposed between the second layer and a device layer of the substrate, and wherein the second wire is a heat source to the first wire at the current density J in the first wire.

[c26] 26.The electronic structure of claim 25, wherein the electrical resistivity of the first wire exceeds the electrical resistivity of the second wire.

[c27] 27. The electronic structure of claim 19, wherein the substrate further

comprises a thermally conductive layer having a thermally conductive member therein and a device layer, wherein the thermally conductive layer is above or below the first layer, wherein the thermally conductive member and the device layer are thermally coupled to each other by a dielectric layer disposed between the first wire and the thermally conductive member and by at least one thermally conductive via disposed between the thermally conductive member and the device layer, wherein the dielectric layer has a sufficiently small thickness in the Y direction that permits conductive heat transfer through the thickness of the dielectric layer, and wherein the thermally conductive member does not carry an electric current.

[c28] 28. The electronic structure of claim 27, wherein the thermally conductive layer is disposed between the first layer and the device layer.

[c29] 29.The electronic structure of claim 27, wherein the first layer is disposed between the thermally conductive layer and the device layer.

[c30] 30. The electronic structure of claim 27, wherein the at least one thermally conductive via is in mechanical contact with a portion of the device layer that does not include an active electronic device.